

~~【書類名】~~

~~図面~~

~~【図1】~~

Fig. 1

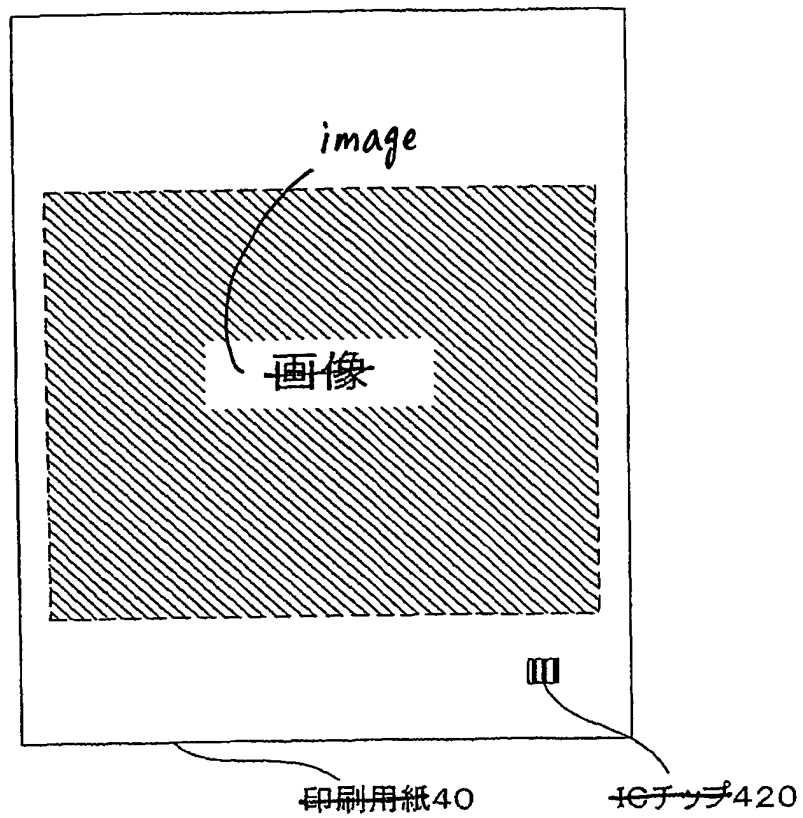
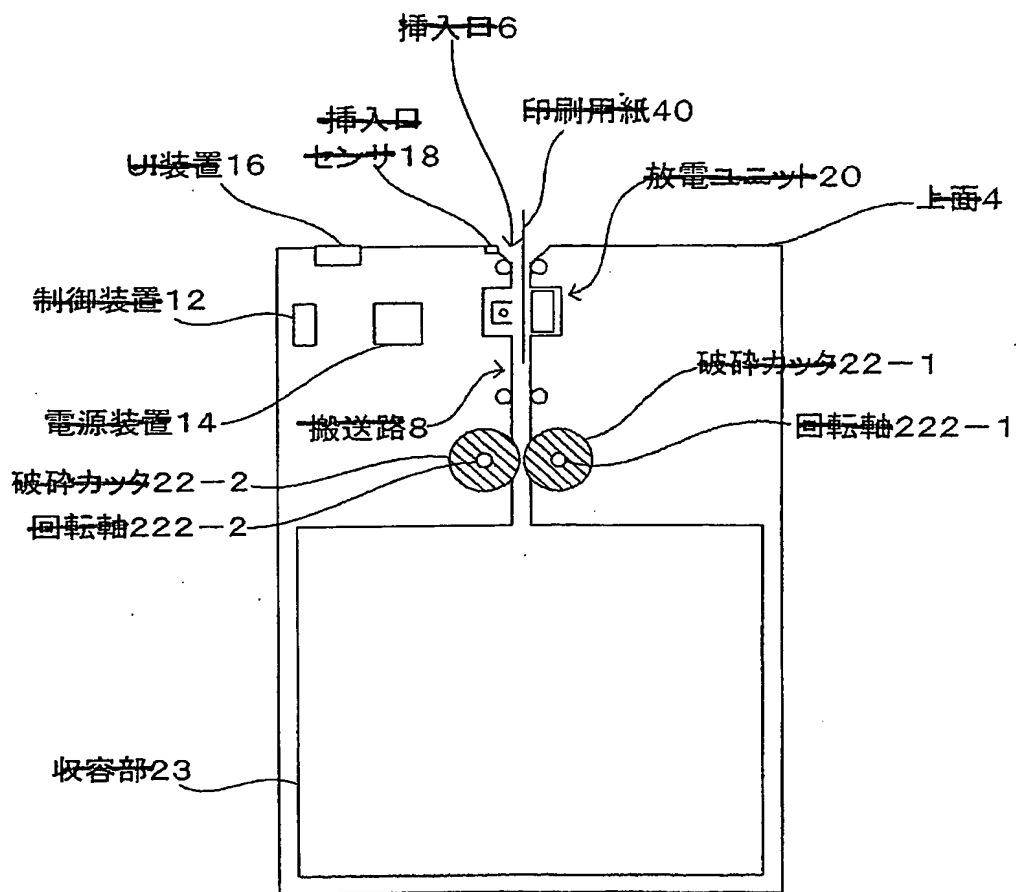


Fig. 2



シヨボツタ2

【図3】

Fig. 3

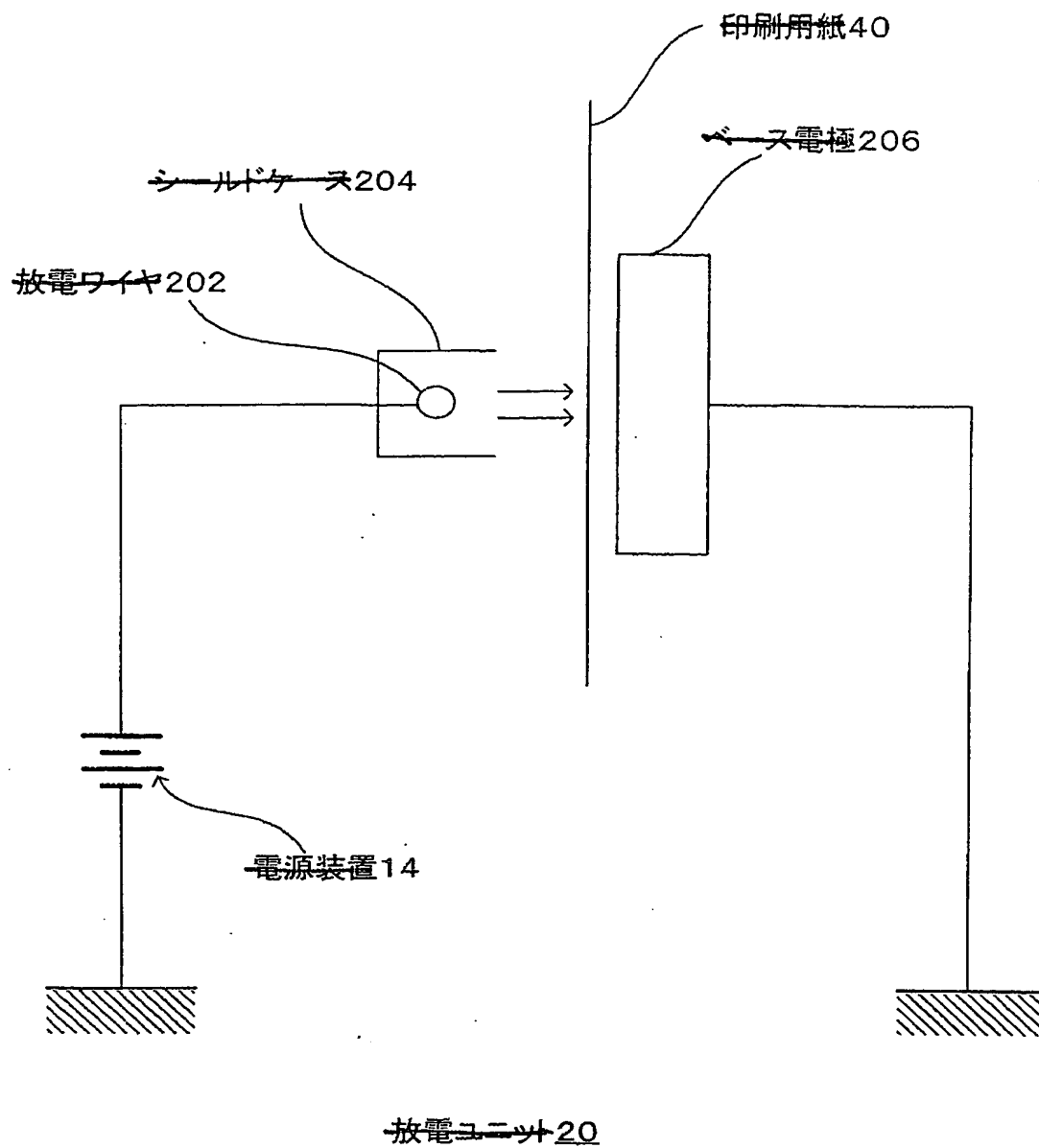
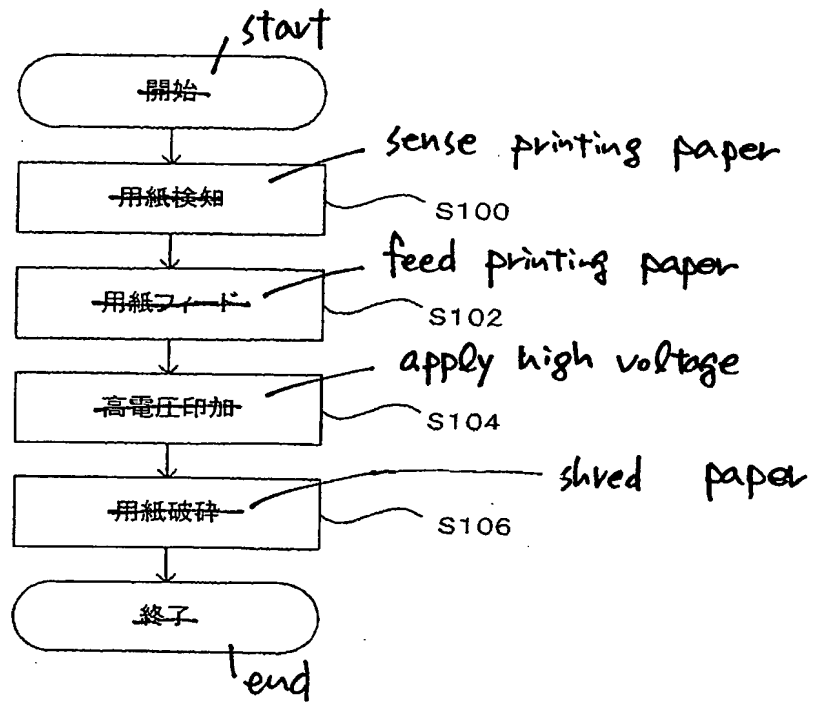
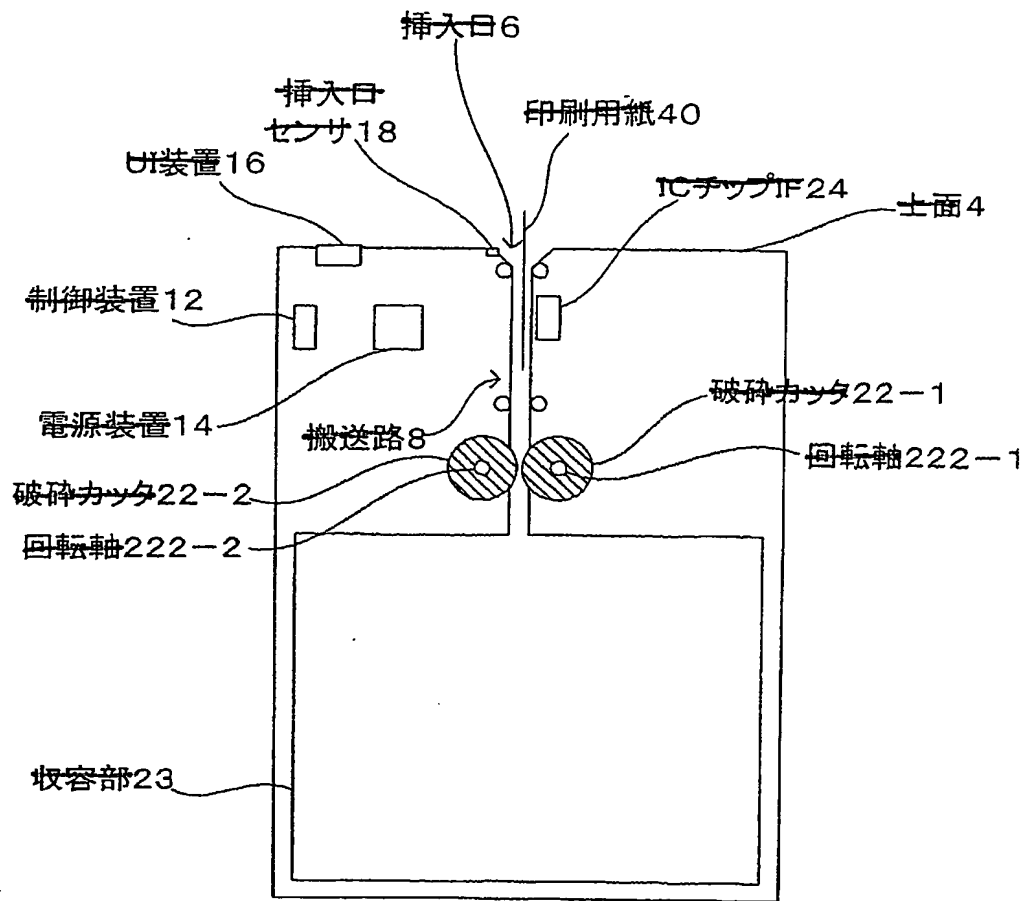


Fig. 4



S10

Fig. 5



シエラフダ金 3

Fig. 6

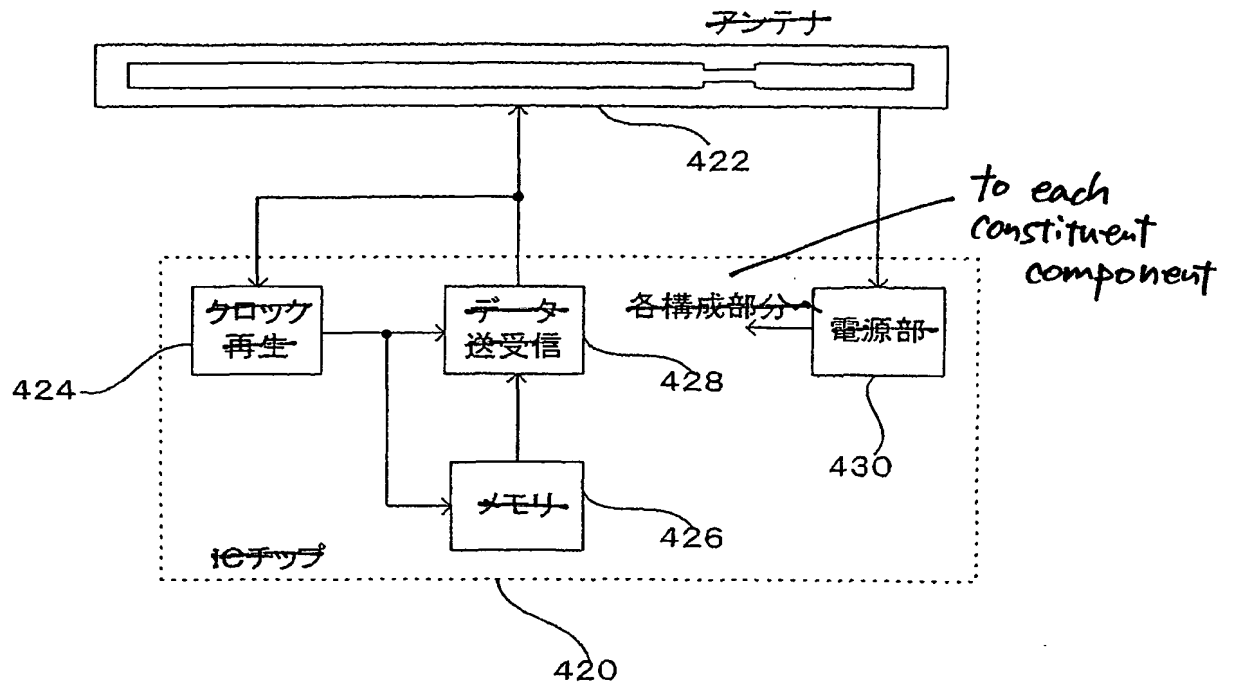


FIG. 6

424 clock reproducing circuit  
428 data transmitting/receiving circuit  
430 power supply circuit  
426 memory circuit

Fig. 7

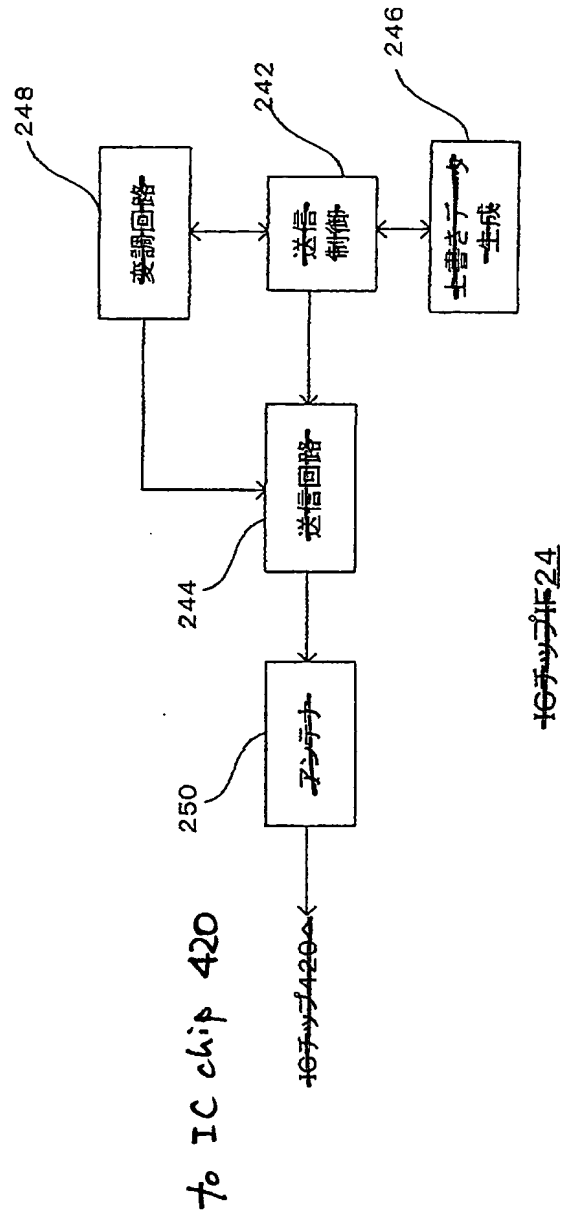




FIG. 7

242 transmission control circuit

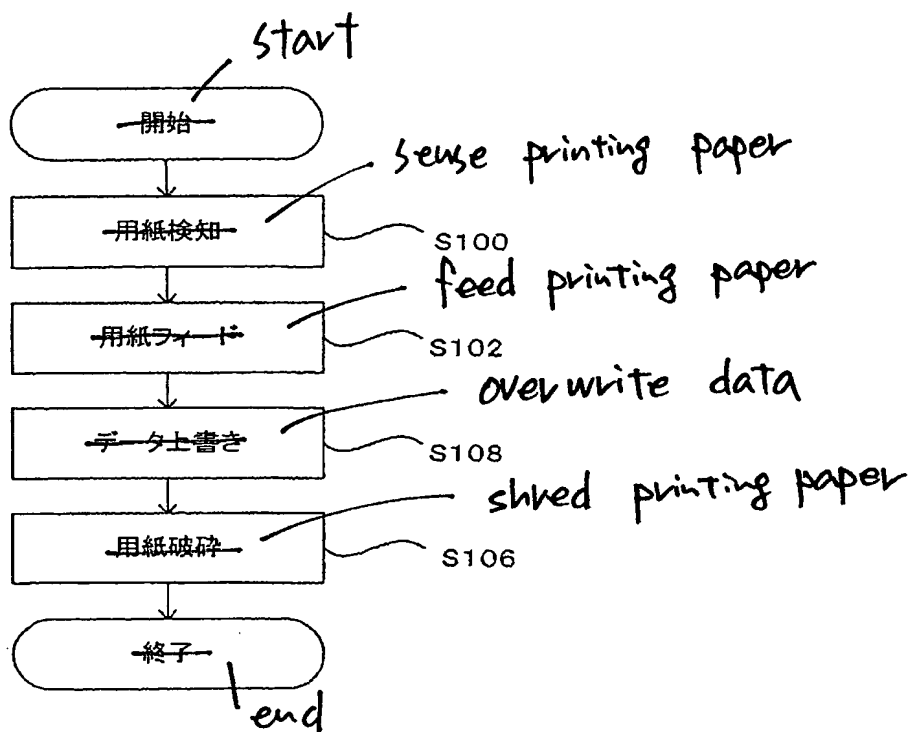
244 transmitting circuit

246 overwritten data producing circuit

248 modulating circuit

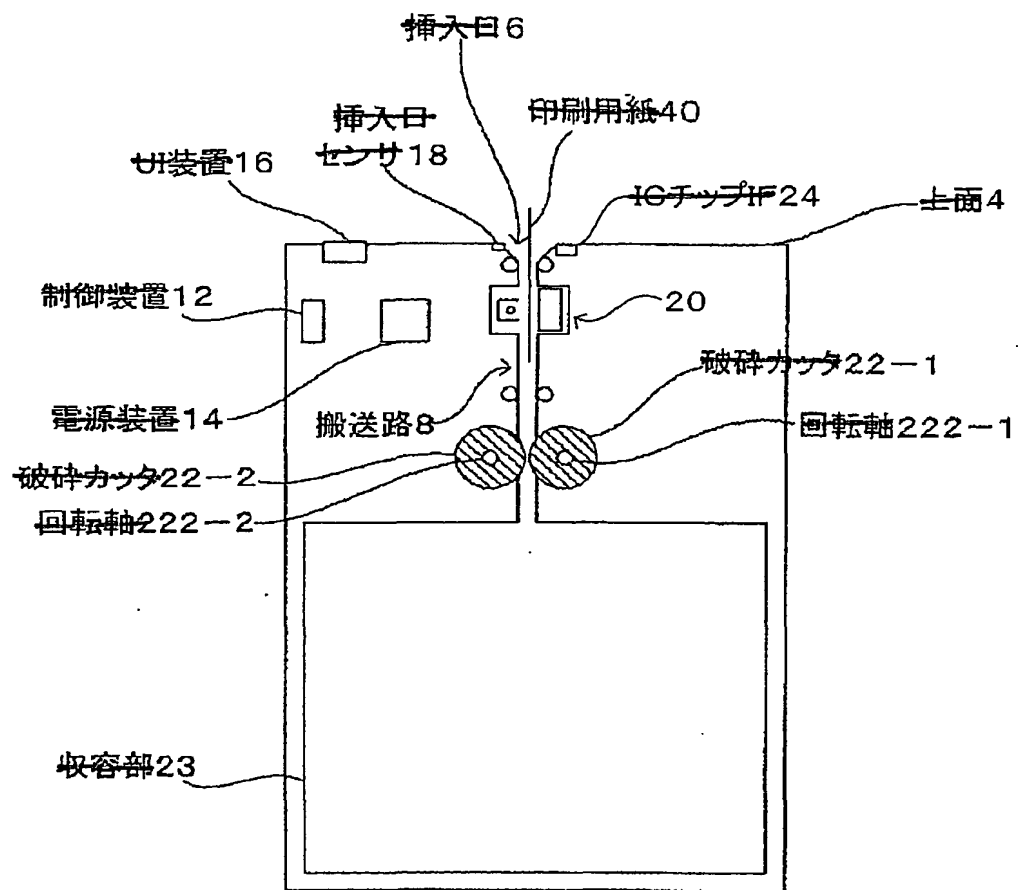
250 antenna

Fig. 8



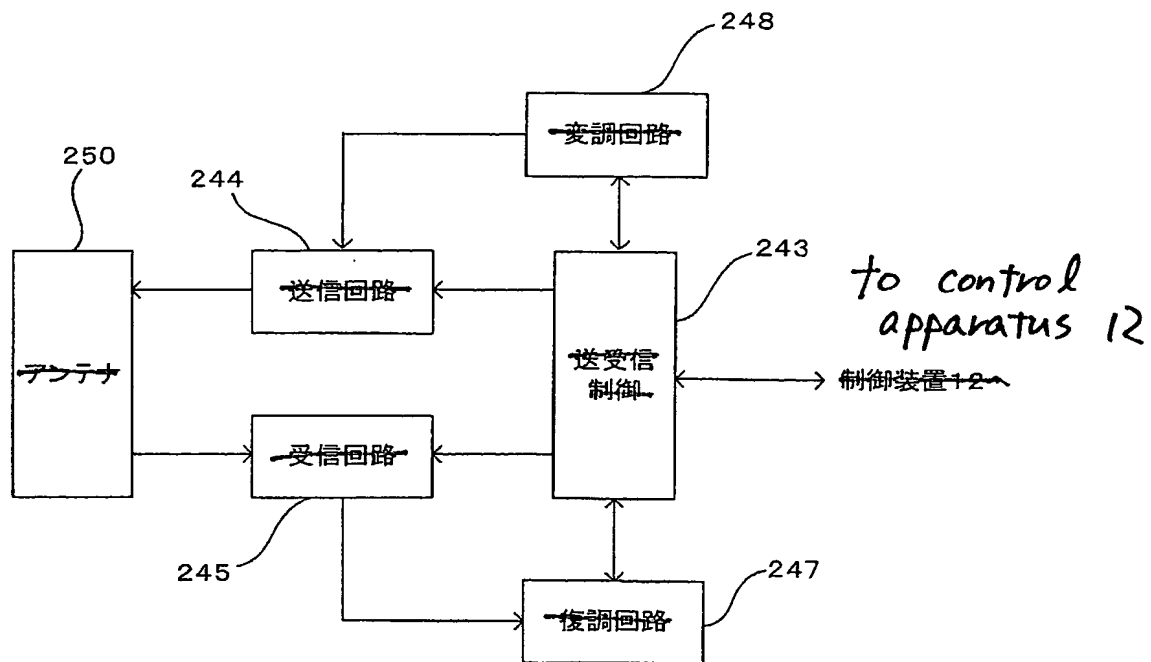
S20

Fig. 9



シミュレーション図5

Fig. 10



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FIG. 10

243 transmission/reception control circuit  
244 transmitting circuit  
245 receiving circuit  
247 demodulating circuit  
248 modulating circuit  
250 antenna